2018

(April)

COMPUTER SCIENCE

(Elective/Honours)

(Digital Logic Design and Computer Architecture)

(CS–201T)

Marks : 75

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **one** question from each Unit

UNIT—I

1. *(a)* Use either 9's complement or 10's complement to perform subtraction of the following decimal numbers : 2

3570 – 2100

(b) Use either 9's complement or 10's complement to perform subtraction of the following decimal numbers : 3

15 – 5800

(Turn Over)

(c) Use either 1's complement or 2's complement to perform subtraction of the following binary numbers : 3

$1000 - 1100$

(d) Convert the decimal number $(5)_{10}$ to base 2. 1

(e) Convert the decimal number $(225)_{10}$ to base 16. 2

(f) Convert the binary number $(1011)_2$ to base 10. 2

(g) Obtain the truth table for the following Boolean function : 2

$F = A \cdot B + A$

2. (a) Explain the following in brief : $1 \times 4 = 4$

(i) 1's complement

(ii) 2's complement

(iii) 9's complement

(iv) 10's complement

(b) Use either 1's complement or 2's complement to perform subtraction of the following binary numbers : 2

$1100 - 1000$

(c) Explain the following in brief : $1+1=2$

(i) Octal number system

(ii) Hexadecimal number system

(Continued)

(d) What are logic gates? Explain. 4

(e) What are universal gates? 3

UNIT—II

3. (a) Simplify the following Boolean expression, given by the function $F(A, B, C, D)$, a function of four variables, viz., A, B, C and D :

$F(A, B, C, D) = \Sigma(1, 2, 3, 5, 6, 7, 13, 14, 15)$

Use a four-variable Karnaugh map. Write the answer in the Sum-of-Products (SOP) form. 5

(b) Show that $(BC' + A'D)(AB' + CD') = 0$. 2

(c) Express the following Boolean expression as a sum of minterms : 2

$F(A, B, C) = 1$

The given function $F(A, B, C)$ uses three variables, viz., A, B and C.

(d) Simplify the following Boolean expression $F(A, B, C)$:

$F(A, B, C) = \Sigma(1, 3, 4, 5, 7)$

$d(A, B, C) = \Sigma(0, 6)$

The given function $F(A, B, C)$ uses three variables, viz., A, B and C. The don't care conditions $d(A, B, C)$ are also given. Use a three-variable Karnaugh map. Write the answer in the Sum-of-Products (SOP) form. 4

(Turn Over)

(e) Draw a logic diagram using only NAND gates to represent the following Boolean expression : 2

$$A \cdot B + C \cdot D$$

4. (a) What is De Morgan's theorem? 2

(b) Define canonical form. 1

(c) Define don't care conditions. 1

(d) Draw a logic diagram for the following Boolean expression : 3

$$(A+B) \cdot (C+D) \cdot (E+F)$$

(e) Convert the following Boolean expression into canonical form : 3

$$F(A, B, C, D) = AB'D + BCD'$$

The given expression is a function $F(A, B, C, D)$; a function of four variables, viz., A, B, C and D. Use all the four variables, viz., A, B, C and D to represent the given function $F(A, B, C, D)$.

(f) Simplify the following Boolean expressions :

$$F(A, B, C) = \Sigma(0, 1, 3, 4, 5, 7)$$

The given function $F(A, B, C)$ uses three variables, viz., A, B and C. Use a three-variable Karnaugh map. Write the answer in the Sum-of-Products (SOP) form. 3

(g) Simplify the following Boolean expression : 2

$$A + A'B + A'B'$$

(Continued)

UNIT—III

5. (a) Show the step-by-step multiplication process using Booth's algorithm for multiplying the following positive numbers :

$$(+15) \times (+13)$$

Assume that 5-bit registers are used. 10

(b) Derive the Boolean expression for the sum of a full-adder. Draw a truth table with A, B and C as the three inputs, and also use S as the output for the sum. 3

(c) How is logical shift right different from logical shift left? 2

6. (a) Draw the flowchart of Booth's multiplication algorithm for multiplying two binary integers in 2's complement representation. Also explain. 4+7=11

(b) Explain half-adder. 4

UNIT—IV

7. (a) Design a 3-bit counter. It goes through the following states, expressed as 3-bit numbers, namely 000, 001, 010, 011, 100, 101, 110 and 111 in binary (i.e., 0, 1, 2, 3, ... up to 7 in decimal). Use any type of flip-flop for the design of the counter. Draw the following : 3+7=10

(i) State diagram

(ii) Excitation table

(b) Explain instruction cycle. 5

(Turn Over)

8. (a) What is a flip-flop? Explain. 8

(b) What is a register? 2

(c) Explain in brief the following addressing modes : 2+3=5

(i) Direct addressing mode

(ii) Indirect addressing mode

UNIT—V

9. (a) Define the following terms : 1+1+2=4

(i) Hit

(ii) Miss

(iii) Hit ratio

(b) Explain the following in brief : 2+2=4

(i) RAM

(ii) Secondary memory

(c) Explain the following mapping procedures with reference to cache memory : 3+4=7

(i) Direct mapping

(ii) Two-way set-associative mapping

(Continued)

10. (a) Answer the following with respect to DMA : 1+4+4=9

(i) What is the full form of DMA?

(ii) Explain DMA.

(iii) Also draw a relevant diagram.

(b) Explain the following modes of data transfer : 3+3=6

(i) Programmed I/O mode of data transfer

(ii) Interrupt-initiated I/O mode of data transfer

(Internal Assessment = 25)

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